

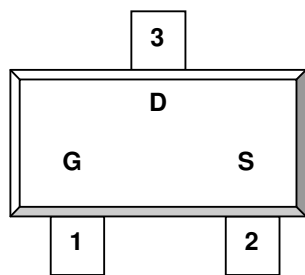
DESCRIPTION

The ST3422A is the N-Channel logic enhancement mode power field effect transistor is produced using high cell density, DMOS trench technology.

This high-density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high side switching.

PIN CONFIGURATION

SOT-23-3L



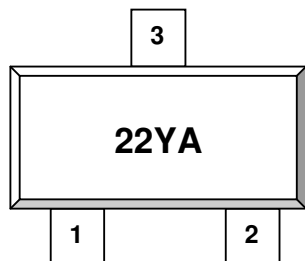
1.Gate 2.Source 3.Drain

FEATURE

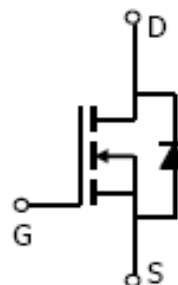
- 60V/6.0A, $R_{DS(ON)} = 28m\Omega$ (Typ.) @ $V_{GS} = 10V$
- 60V/2.5A, $R_{DS(ON)} = 38m\Omega$ @ $V_{GS} = 4.5V$
- 60V/1.5A, $R_{DS(ON)} = 100m\Omega$ @ $V_{GS} = 2.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design

PART MARKING

SOT-23-3L



Y: Year Code A: Week Code





ST3422A 

N Channel Enhancement Mode MOSFET

6.0A

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	60	V
Gate-Source Voltage		V _{GSS}	±20	V
Continuous Drain Current (T _J =150°C)	T _A =25°C T _A =70°C	I _D	6.0 4.6	A
Pulsed Drain Current		I _{DM}	20	A
Continuous Source Current (Diode Conduction)		I _S	1.7	A
Power Dissipation	T _A =25°C T _A =70°C	P _D	2.0 1.3	W
Operation Junction Temperature		T _J	-55/150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		R _{θJA}	75	°C/W



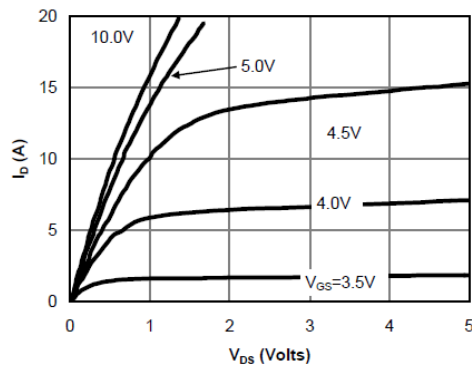
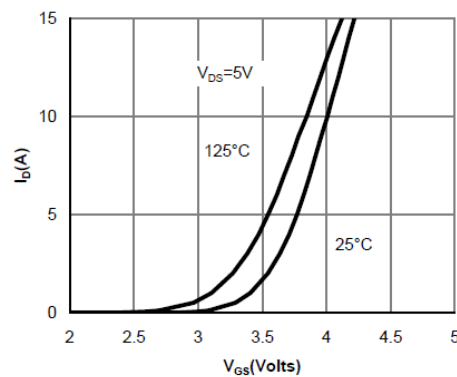
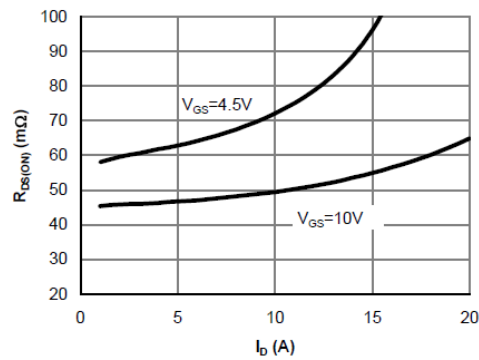
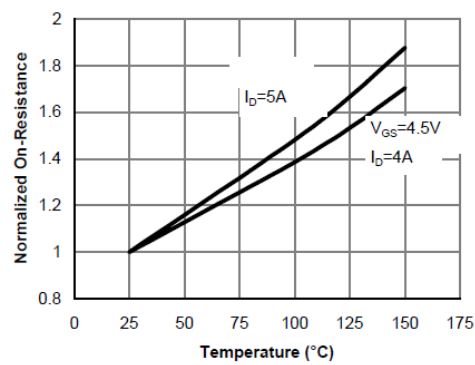
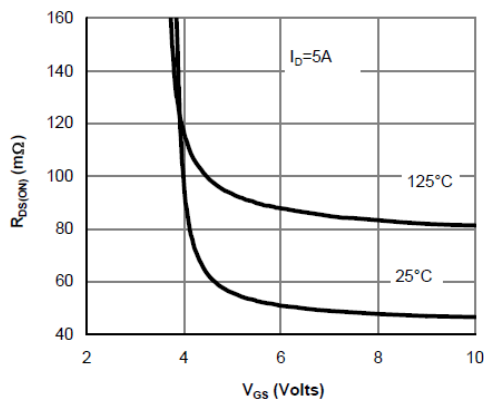
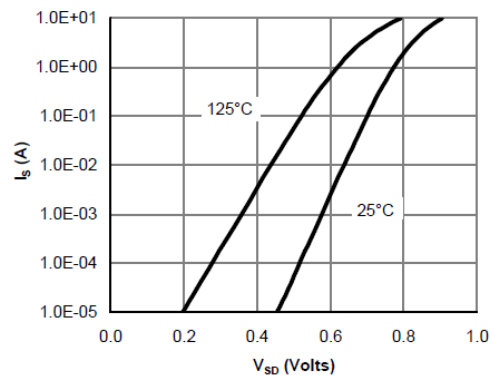
ST3422A 

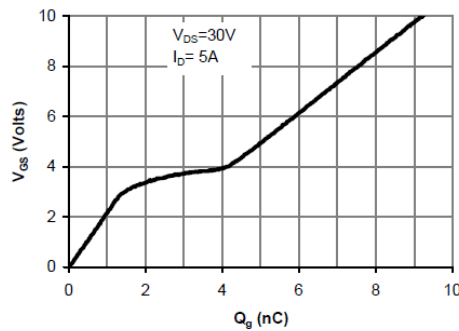
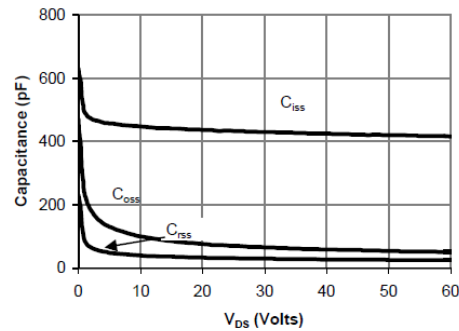
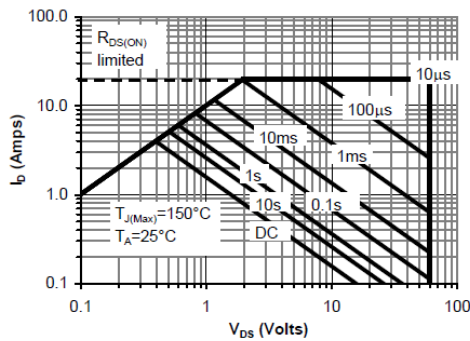
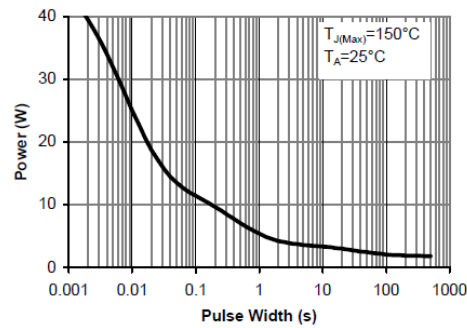
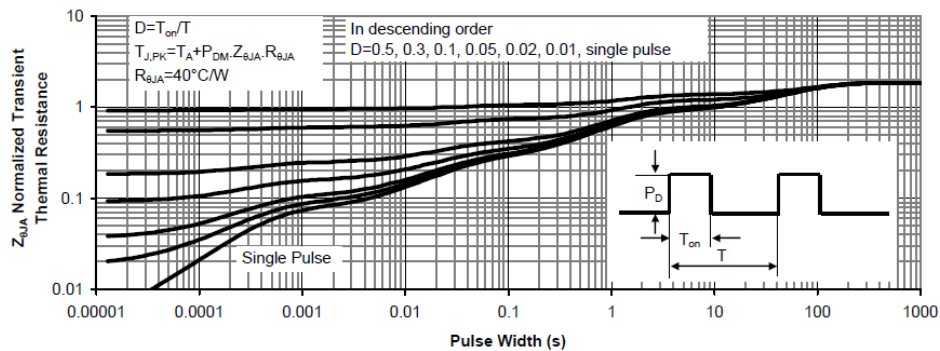
N Channel Enhancement Mode MOSFET

6.0A

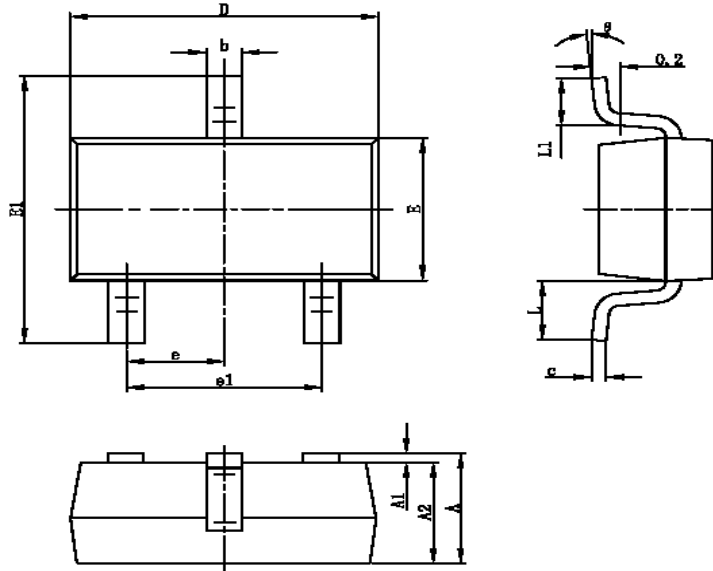
ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250uA	60			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1		3	V
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =48V, V _{GS} =0V			1	uA
		V _{DS} =48V, V _{GS} =0V T _J =55℃			10	
Drain-source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =6.0A V _{GS} =4.5V, I _D =2.5A V _{GS} =2.5V, I _D =1.5A		28 38 100		mΩ
Forward Transconductance	g _{fs}	V _{DS} =4.5V, I _D =5.8A		11		S
Diode Forward Voltage	V _{SD}	I _S =1.7A, V _{GS} =0V			1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =15V V _{GS} =10V I _D ≐6.7A		10	22	nC
Gate-Source Charge	Q _{gs}			1.8		
Gate-Drain Charge	Q _{gd}			3.8		
Input Capacitance	C _{iss}	V _{DS} =15V V _{GS} =0V F=1MHz		455		pF
Output Capacitance	C _{oss}			243		
Reverse Transfer Capacitance	C _{rss}			38		
Turn-On Time	t _{d(on)} tr	V _{DD} =15V R _L =15Ω I _D =1.0A V _{GEN} =10V R _G =6Ω		8	15	nS
Turn-Off Time	t _{d(off)} tf			10	20	
				20	40	
				11	20	

TYPICAL CHARACTERISTICS (25°C Unless noted)

Fig 1: On-Region Characteristics

Figure 2: Transfer Characteristics

Figure 3: On-Resistance vs. Drain Current and Gate Voltage

Figure 4: On-Resistance vs. Junction Temperature

Figure 5: On-Resistance vs. Gate-Source Voltage

Figure 6: Body-Diode Characteristics

TYPICAL CHARACTERISTICS (25°C Unless noted)

Figure 7: Gate-Charge Characteristics

Figure 8: Capacitance Characteristics

Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

Figure 11: Normalized Maximum Transient Thermal Impedance

SOT-23-3L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°